Analog and Digital Electronic Circuit Laboratory Manual
3rd Sem, B.Tech. (Electrical Engineering)

Department of Electrical Engineering
Veer Surendra Sai University of Technology Burla

VISION

To be recognized as a centre of excellence in education and research in the field of Electrical Engineering by producing innovative, creative and ethical Electrical Engineering professionals for socio-economic development of society in order to meet the global challenges.

MISSION

Electrical Engineering Department of VSSUT Burla strives to impart quality education to the students with enhancement of their skills to make them globally competitive through:

M1. Maintaining state of the art research facilities to provide enabling environment to create, analyze, apply and disseminate knowledge.

M2. Fortifying collaboration with world class R&D organizations, educational institutions, industry and alumni for excellence in teaching, research and consultancy practices to fulfil 'Make in India' policy of the Government.

M3. Providing the students with academic environment of excellence, leadership, ethical guidelines and lifelong learning needed for a long productive career.

PROGRAM EDUCATIONAL OBJECTIVES of B.Tech. (EE)

The program educational objectives of B.Tech. in Electrical Engineering program of VSSUT Burla are to prepare its graduates:

1. To have basic and advanced knowledge in Electrical Engineering with specialized knowledge in design and commissioning of electrical systems/renewable energy systems comprising of generation, transmission and distribution to become eminent, excellent and skillful engineers.
2. To succeed in getting engineering position with electrical design, manufacturing industries or in software and hardware industries, in private or government sectors, at Indian and in Multinational organizations.
3. To have a well-rounded education that includes excellent communication skills, working effectively on team-based projects, ethical and social responsibility.
4. To have the ability to pursue study in specific area of interest and be able to become successful entrepreneur.
5. To have broad knowledge serving as foundation for lifelong learning in multidisciplinary areas to enable career and professional growth in top academic, industrial and government/corporate organizations.

List of experiments analog and digital electronic circuit lab

1. Determination of the frequency response of Low pass filters.
2. Determination of the frequency response of High pass filters.
3. Study of output characteristics of FET.
4. Analysis of BJT biasing circuits.
5. RC phase shift oscillator and to observe its output waveform.
6. Realization of half-adder, full-adder, half-subtractor and full-subtractor.
7. Design and implementation of multiplexer and demultiplexer.
8. Realization of S-R and J-K flip flop using 7400.
9. Design of 3-bit asynchronous counter and Mod-N counter.
10. Design of SISO, SIPO, PISO, PIPO shift registers.

Course Outcomes:

After completion of this laboratory course the students will be able to

CO1	Know about the MATLAB software and its application in DC, single phase and three phase electric circuit to analyze.
CO2	Extend understanding for solving other electrical problems using the software.
CO3	The students can interpret and summarize from the response the type of the system.
CO4	Discover how to apply the different numerical techniques for analysis of electrical systems and its implementation with MATLAB.
CO5	Modify circuit simulation in different ways by both programming and Simulink blocks in MATLAB.

Experiment no.: 01

1.1 Aim of the Experiment:

Determination of frequency response of Low Pass Filter.

1.2 Apparatus required:

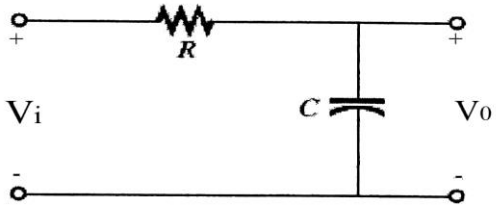
- Audio signal generator
- AC/DC mil voltmeter / VTVM
- Resistor
- Capacitor

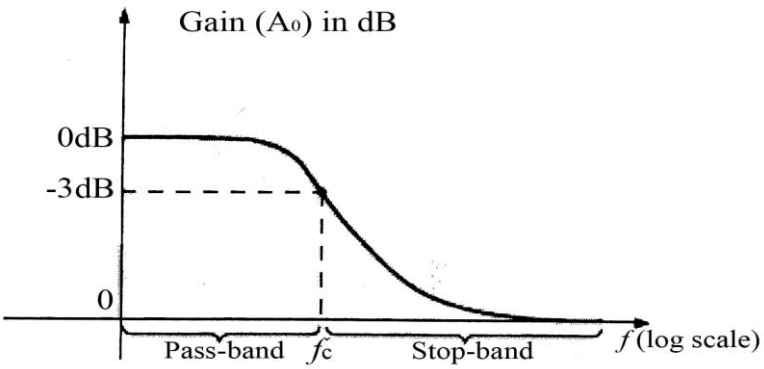
1.3 Theory:

LPF:

A LPF is one that passes all frequencies below a selected value f_c and attenuates higher frequencies. Such a filter can be realized by a series 'R' and shunt 'C' as shown below. Its frequency response curve is also shown.

3dB cut-off frequency $f_c = 1/2\pi RC$





1.4 Procedure:

a) Choose f_c anywhere between 1 KHz to 10KHz.
b) Choose the value of 'C' between 0.01μF to 0.1μF.
c) Calculate 'R'. Connect R and C as shown.
d) Connect the Audio signal generator at the input of the HPF.
e) Keeping input voltage at 1V sine wave, measure the output voltage of HPF by AC/DC mill voltmeter.
f) Take the output reading for different frequencies from 20Hz to 20KHz keeping input constant.
g) Plot the frequency response curve (frequency Vs. Gain) and verify f_c.

1.5 Tabulation:

Sl. No.	Input Voltage	Frequency	Output Voltage	Gain

1.6 Conclusion:

Experiment no.: 02

2.1Aim of the Experiment:

Determination of frequency response of High Pass Filter.

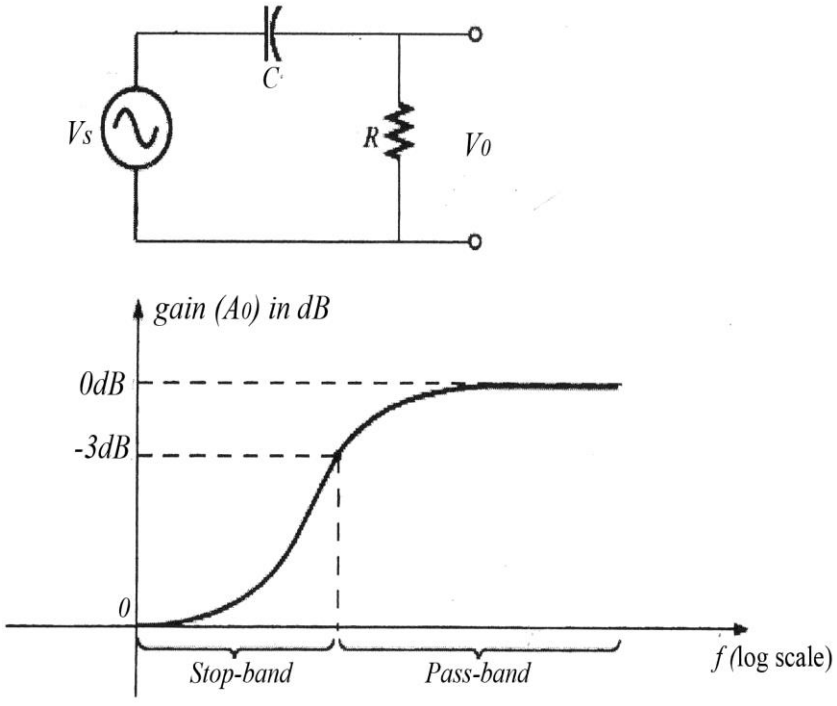
2.2 Apparatus required:

- Audio signal generator
- AC/DC mil voltmeter / VTVM
- Resistor
- Capacitor

2.3Theory:

HPF:

A HPF is one that passes all frequencies above a selected value f_c and attenuates lower frequencies. Such a filter can be realized by a series 'C' and shunt 'R' as shown below. Its frequency response curve is also shown. 3dB cut-off frequency $f_c = 1/2\pi RC$



2.4 Procedure:

a) Choose f_c anywhere between 1 KHz to 10KHz.

b) Choose the value of 'C' between 0.01μF to 0.1μF.

c) Calculate 'R'.

d) Connect R and C as shown.

e) Connect the Audio signal generator at the input of the HPF.

f) Keeping input voltage at 1V sine wave, measure the output voltage of HPF by Decade resistance box.

g) Take the output reading for different frequencies from 20Hz to 20KHz keeping input constant.

h) Plot the frequency response curve (frequency Vs. Gain) and verify f_c.

2.5 Tabulation:

Sl. No.	Input Voltage	Frequency	Output Voltage	Gain

2.6 Conclusion:

Experiment no.: 03

3.1 Aim of the Experiment:

Study of output characteristics of FET.

3.2 Apparatus required:

- Lab FET characteristic Trainer
- Digital Multimeter
- Ammeter (0-5) mA
- Set of patching wires.

3.3 Theory:

The junction FET (also called a JFET) finds many applications in electronic circuits. This device is constructed from N-type and P-type semiconductor materials and like the conventional bipolar transistor it is capable of amplifying electronic signals. However, the junction FET is constructed in a different manner than a bipolar transistor and the device operates on an entirely different principle.

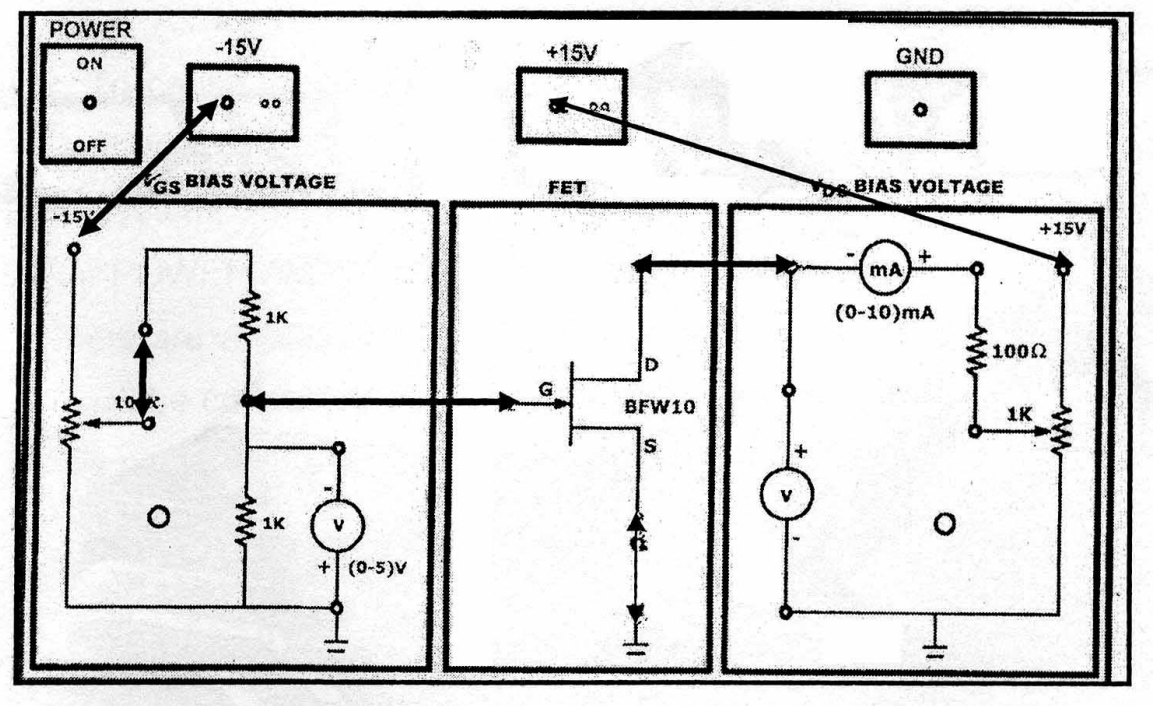


Fig 3.1 WIRING DIAGRAM FET CHARACTERISTICS

3.4 Procedure:

a) Patch the circuit as shown in wiring diagram.

b) Apply – 15 volts DC voltage to the 100 k potentiometer (designated as R_1). You will be using this potentiometer to control the voltage applied to 1000-ohm resistors R_2 and R_3 that are in series. These to resistors divide the voltage taken from R_1 in half. The reduced voltage that appears across R_3 serves as the gate-to-source bias voltage (V_{GS}) for the FET.

c) Switch ON the trainer. Apply +15 volts DC voltage to 1000 ohm potentiometer R_5. You will be using this potentiometer to control the drain-to-source voltage (V_{GS}) applied to the FET. The drain current (l_D) flowing through the FET must pass through 100ohm resistor R_4. As you proceed through this experiment you will periodically measure the voltage across R_4 and then use Ohm's law to calculate l_D.

d) Turn potentiometers R_1 and R_5 fully clockwise and then turn on your trainer.

e) Leave potentiometers R_1 fully counter clockwise so that gate-to-source voltage (V_{GS}) applied to the FET will be zero. Adjust potentiometers R_5 until the drain-to-source voltage (V_{DS}) is equal to 1 volt (measure this voltage with your voltmeter).

f) Now use your voltmeter to measure the voltage across R_4. Use this voltage reading and the resistance of R_4 (100 ohms) to calculate the FET's drain current (l_D) according to Ohm's law.

g) Record your calculated l_D value (in miliamperes) immediately below the V_{DS} value of 1 volt in the table provided in Table-1.

h) Now complete the table-1 by adjusting V_{DS} to the remaining values indicated and record the corresponding values of l_D. To do this, simply repeat steps 4 and 5 above for each value of V_{DS} indicated. When you complete the table-1 you will have a permanent record of l_D, values over a range of V_{DS} values when V_{GS} is equal to zero.

i) Now adjust potentiometer R_1 so that V_{GS} is equal to 0.25 volts (measure with your voltmeter).

j) Without disturbing the setting of R_1, adjust potentiometer R_5 until V_{DS} is equal to 1 volt (measure V_{DS} with your voltmeter).

k) Now use your voltmeter to measure the voltage across R_4. Use this voltage reading and the resistance of R_4 (100 ohms) to calculate l_D according to Ohm's law. Record your calculated l_D value (in miliamperes) immediately below the V_{DS} value of volt in the Table-1.

l) Now complete the Table-1 by adjusting V_{DS} to the remaining values indicated and recording the corresponding values of l_D. To do this, simply repeat steps 8 and 9 above for each value of V_{DS} indicated. When you complete the table – 2, you will have a

record of l_D values over a range of V_{DS} values when V_{GS} is equal to – 0.25 volts. A negative sign is placed before the V_{GS} value to indicate that the gate is negative with respect to the source.

m) Now prepare the tables for the values of VGS = -0.5, 0.75 as explained as in the above procedure.

n) Now use the corresponding values of V_{DS} and l_D that you recorded in Table-1 to plot the drain characteristic curves on the graph shown in Figure-4. Connect the various points plotted to form a continuous curve. Label this curve $V_{GS} = 0$.

o) Use the corresponding values of V_{DS} and l_D, plot a curve on the graph of Figure 4 for each value of V_{GS}.

p) Now use the set of drain characteristic curves that you plotted in Figure-4 to determine the transconductance of the FET. Select a constant value of V_{DS} that is well above the pinch-off voltage (V_P) of the device (possibly 6 or 7 volts) and observe the change in l_D when V_{GS} changes from 0 to -0.25 volts. This will insure that you transconductance value will be measured in the pinch-off region of the device. Use the transconducance equation given below and record your results in the space provided below:

q) Transconductance = $\dfrac{\Delta / D}{\Delta V_{GS}}$

3.5 Tabulation:

V_{GS} = 0		**V_{GS}**		**V_{nS}**		**$V_{GS} = V_p$**	
V_{DS}	**l_D**	**V_{DS}**	**l_D**	**V_{DS}**	**l_D**	**V_{DS}**	**l_D**

3.6 Conclusion:

Experiment no.: 04

4.1 Aim of the Experiment:

Analysis of BJT biasing circuits.

4.2 Apparatus required:

- BJT Biasing Trainer Kit
- Multi meter
- Patch chords

4.3 Theory:

Bipolar transistor amplifier must be properly biased to operate correctly. In circuits made with individual devices (discrete circuits), biasing networks consisting of resistor are commonly employed. Much more elaborate biasing arrangements are used in integrated circuits. The voltage divider configuration achieves the correct voltages by the use of resistors in certain patterns. By manipulating the resistors in certain ways you can active more stable current levels without having value affect it too much

The operating point of a device, also known as bias point, quiescent point, or Q-point, is the point on the output characteristics that shows the DC collector-emitter voltage (F_{m}) and the collector current (I_{c}) with no input signal applied. The term is normally used connection with devices such transistor.
At constant current, the voltage across the emitter-base junction V RU of a bipolar transistor decreases 2 mV (silicon) and 1.8mV (germanium) for each T deg * C in temperature (reference being 25 deg * C) By the Ebers-mole model, if the base-emitter voltage V H i is held constant and the temperature rises, the current through the base emitter diode I_{0} will increase, and thus the collector current L_{C} will also increase. Depending on the bias point, the power dissipated in the transistor may also increase, which will further increase its temperature and exacerbate the problem. This deleterious positive feedback results in thermal ninway. There are several approaches to mitigate bipolar transistor thermal runaway.

FIXED BIASING

This form of biasing is also called base bias or fixed resistance biasing. In the circuit a single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used.
In the given circuit,

$$V_{cc} = I_B R_B + V_{bc}$$

Therefore,

$$V_{bc} = V_{cc} - I_B R_B$$

and

$$I_B = (V_{cc} - V_{bc})/R_B$$

For a given transistor, V_{bc}does not vary significantly during use. As V_{cc}, is of fixed value, on selection of R_B, the base current I_B is fixed. Therefore, this type is called fixed bias type of circuit.

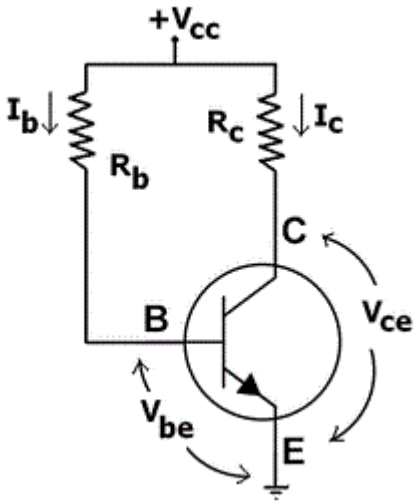
Also for given circuit,

$V_{cc} = I_C R_C + V_{cc}$

Therefore,

$$V_{cc} = V_{cc} - I_C R_C$$

The common-emitter current gain of a transistor is an important parameter in circuit design. and is specified on the data sheet for a particular transistor. It is denoted as ß(hfe) on this page



FEEDBACK BIASING

This configuration employs negative configuration to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor Rb(RB3 or RB4) is connected to the collector instead of connecting it to the DC source Vec. So any thermal runaway will induce a voltage drop across the Re(RC3 or RC4jresistor that will throttle the transistor's hate current.

From kirchhoff's voltage law, the voltage Vrb across the base resistor Rb is

$$V_{R_b} = V_{cc} - (I_c + I_b)R_c - V_{be}$$

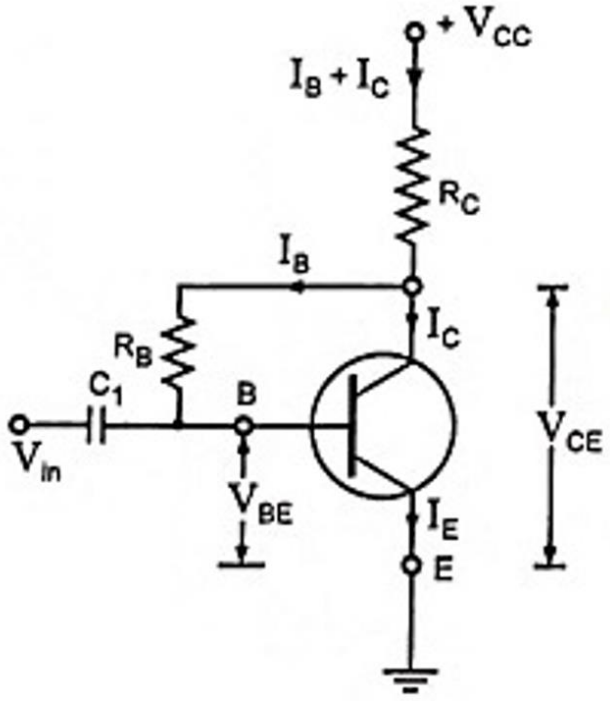
From Ohms law, the base current $I_b = V_{rb}/R_b$, and so

$$I_b R_b = V_{cc} - I_b(\beta + 1)R_c - V_{be}$$

Hence, the base current Ib is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If Vbe is held constant and temperature increases, then the collector current le increases. However, a larger le causes the voltage drop across resistor Re to increase, which in turn reduces the voltage Vrb across the base resistor Rb. A lower base-resistor voltage drop reduces the base current Ib, which results in less collector current le. Because an increase in collector current with temperature is opposed, the operating point is kept stable.



VOLTAGE DIVIDER BIASING

The voltage divider is formed using external resistors R_1(RB5 or RB6) and R_2(RB7 or RB8). The voltage across R_2 forward biases the emitter junction. By proper selection of resistors R_1 and R2, the operating point of the transistor can be made independent of ß. In this circuit. the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point. similar to the below circuits with emitter resistor. The voltage divider configuration achieves the correct voltages by the use of resistors in certain patterns. By manipulating the resistors in certain ways you can achieve more stable current levels without having ß value affect it too much.

In this circuit the base voltage is given by:

$$V_b = voltage\ across\ R_2 = V_{cc}\frac{R_2}{R_1 + R_2} - I_b\frac{R_1 R_2}{R_1 + R_2}$$

For the given circuit,

$$I_B = \frac{\frac{V_{cc}}{1 + R_1/R_2} - V_{be}}{(\beta + 1)R_E + R_1||R_2}$$

4.4 Procedure:

For Fixed Biasing

a) Construct circuit for fixed bias using patch chords.
b) Turn ON the power supply.
c) Measure Ib, Ic, Vbc, Vce values.
d) Record them in the table.
e) Compute the values of the quantities measured and compare it to the measured values.

For Feedback Biasing

a) Construct circuit for feedback bias using patch chords.
b) Turn ON the power supply.
c) Measure Ib, Ic, Vbe, Vce values.
d) Record them in the table.
e) Compute the values of the quantities measured and compare it to the measured values.

For Voltage Divider Biasing

a) Construct circuit for voltage divider bias using patch chords.
b) Turn ON the power supply.
c) Measure Ib, Ic, Ie, Vbe, Vce values.
d) Record them in the table.
e) Compute the values of the quantities measured and compare it to the measured values.

4.5 Tabulation:

For Fixed Bias

Sl No.	Rb	Rc	Ib measured	Ib computed	Ic measured	Ic computed	Ie measured	Ie computed	Vbe measured	Vbe computed	Vce measured	Vce computed

For Feedback Bias

Sl No.	Rb	Rc	Ib measured	Ib computed	Ic measured	Ic computed	Ie measured	Ie computed	Vbe measured	Vbe computed	Vce measured	Vce computed

For Voltage Divider Bias

Sl No.	Rb	Rc	Ib measured	Ib computed	Ic measured	Ic computed	Ie measured	Ie computed	Vbe measured	Vbe computed	Vce measured	Vce computed

4.6 Calculation:

4.7 Conclusion:

Experiment no.: 05

5.1 Aim of the Experiment:

To study RC phase shift oscillator and to observe its output waveform.

5.2 Apparatus required:

- LAB RC Phase Shift Oscillator Trainer.
- Dual Trace Oscilloscope (CRO).
- Set of patching wires

5.3 Theory:

Any circuit which is used to generate a.c. voltage without a,c, input signal is called an oscillator to generate ac voltage, the circuit is supplied energy from a d.c. Source. If the output voltage is a sine wave function of time, the oscillator is called sinusoidal oscillator or Harmonic oscillator Positive feedback and negative resistance oscillator belong to this category.

BARKHAUSEN CRITERION CONDITION FOR OSCILLATION

The oscillator can be described by a positive (or regenerative) feedback system using the block diagram. A frequency -selective feedback network is used, and the oscillator is designed to produce an output even though the input is zero.

For a sinusoidal oscillator, we want the poles of the closed-loop amplifier to be located at a frequency 00, precisely on the jo axis. These circuits use positive feedback through the frequency selective feedback network to ensure sustained oscillation at the frequency 60. Consider the feedback system which is described by

Av =A(s)/ [1-A(s)ß(s)]

=A(s)/ [1-T(s)]

The use of positive feedback results in the minus sign in the denominator. For sinusoidal oscillations, the denominator for Equation (1) must be zero for a particular frequency 0 on the jo axis:

1-T($j\omega$)=0 or T($j\omega$)= +1

The Barkhausen criteria for oscillation are a statement of the two conditions necessary to satisfy the Equation

1. T(jω) = 0 or even multiple of 360 degree
2. T($j\omega$) |=1

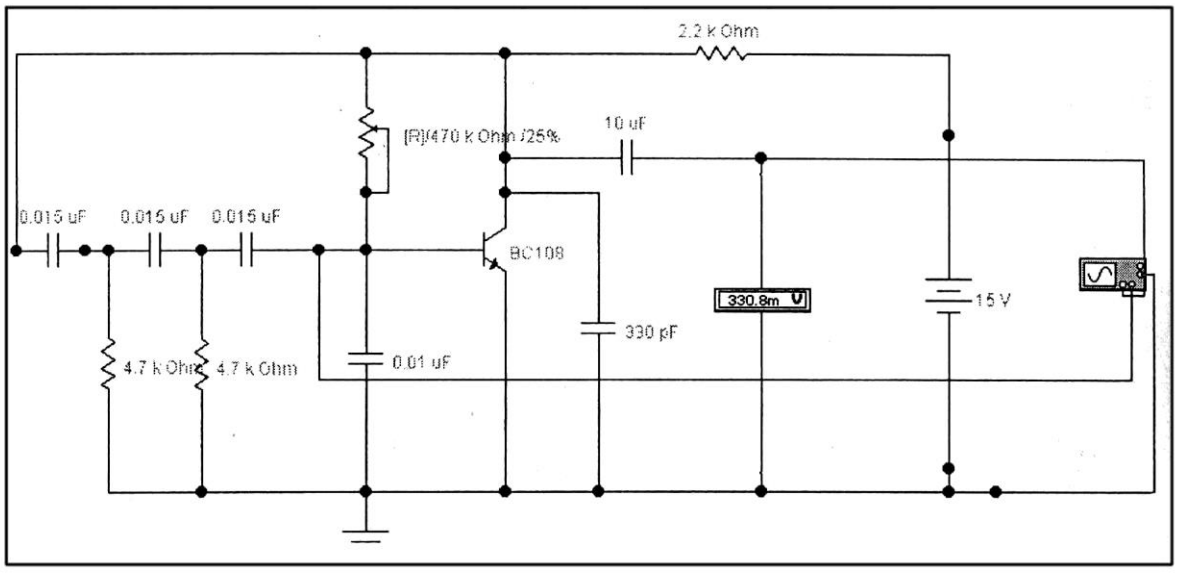
These two criteria state that the phase shift around the feedback loop must be zero degrees, and the magnitude of the loop gain must be unity. Unity loop gain corresponds to a truly sinusoidal oscillator. A loop gain greater than I causes distorted oscillation to occur.

RC OSCILLATORS

All the oscillators using tuned LC circuits operate well at high frequencies. At low frequencies, as the inductors and capacitors required for the time circuit would be very bulky, RC oscillators are found to be more suitable. Two important RC oscillators are (1) RC Phase shift oscillator and (ii) Wien Bridge oscillator.

RC PHASE SHIFT OSCILLATOR

In this oscillator the required phase shift of 180 degree in the feedback loop from output to input is obtained by using R and C components instead of tank circuit. The circuit diagram shows the circuit of RC phase shift oscillator. Here, a common emitter amplifier is followed by three sections of RC phase shift network, the output of the last section being returned to the input. In order to make the three RC sections identical, R3 is chosen as R3R-Ri is the input impedance of the circuit. If the values of R and C are chosen so that, for the given frequency f the phase shift of each RC section is 60 degree. Thus such a RC ladder network produces a total shift of 180 degree between its input and output voltages for only the given frequency. Therefore, at the specific frequency f the total phase shift from the base of the transistor around the circuit and back to the base will be exactly 360 degree or 0 degree; thereby satisfying Barkhausen condition for oscillation. The frequency of oscillation is given by $F = 1/(2\pi RC\sqrt{6})$. At this frequency, it is found that the feedback factor of the network is B-1/29 oscillation operation. In order that [Aß| shall not be less than unity, it is hon required that the amplifier gain must be more than 29 for oscillator operation. The RC phase shift oscillator is suitable for audio frequencies only. Its main drawbacks are that the three capacitors or resistors should be changed simultaneously to change the frequency of oscillation and it is difficult to control the amplitude of oscillation without affecting the frequency of oscillation.



Circuit diagram of RC-Phase Shift Oscillator

5.4 Procedure:

a) Take the trainer for RC Phase Shift Oscillator and connect it to 220V AC power supply.
b) Connect points A to B, C to D and F to G.
c) Switch ON the instrument.
d) Connect the output signal of RC Phase Shift Oscillator at CRO using CRO probe.
e) Measure the frequency at the oscillator output.
f) Measure the output voltage at the oscillator out put.
g) Now connect C to E and measure the frequency.
h) Similarly take different combinations of the resistors and see the effect.

5.5 Conclusion:

Experiment no.: 06

6.1 Aim of the Experiment:

To design and construct half adder, full adder, half subtractor and full subtractor circuits and verify the truth table using logic gates.

6.2 Apparatus required:

SL No.	COMPONENT	SPECIFICATION	QTY
1.	AND GATE	IC 7408	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
4.	X-OR GATE	IC 7486	1
5.	IC TRAINER KIT	-	1
6.	Patch Chords		AS REQUIRED

6.3 Theory:

HALF ADDER:

A half adder has two inputs for the two bits to be added and two outputs one from the sum 'S' and other from the carry 'c' into the higher adder position. Above circuit is called as a carry signal from the addition of the less significant bits sum from the X-OR Gate the carry out from the AND gate.

FULL ADDER:

A full adder is a combinational circuit that forms the arithmetic sum of input; it consists of three inputs and two outputs. A full adder is useful to add three bits at a time but a half adder cannot do so. In full adder sum output will be taken from X-OR Gate, carry output will be taken from OR Gate.

HALF SUBTRACTOR:

The half subtractor is constructed using X-OR and AND Gate. The half subtractor has two input and two outputs. The outputs are difference and borrow. The difference can be applied using X-OR Gate, borrow output can be implemented using an AND Gate and an inverter.

FULL SUBTRACTOR:

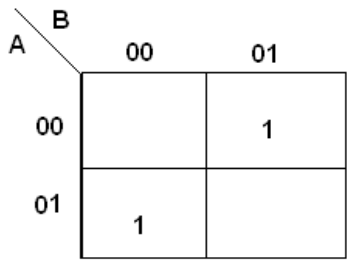
The full subtractor is a combination of X-OR, AND, OR, NOT Gates. In a full subtractor the logic circuit should have three inputs and two outputs. The two half subtractor put together gives a full subtractor .The first half subtractor will be C and A B. The output will be difference output of full subtractor. The expression AB assembles the borrow output of the half subtractor and the second term is the inverted difference output of first X-OR.

HALF ADDER

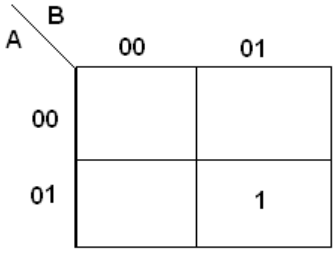
TRUTH TABLE:

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

K-Map for SUM:



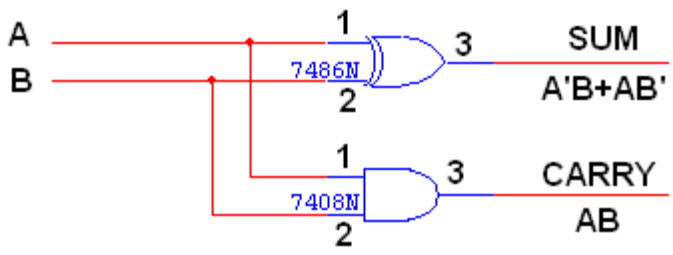
K-Map for CARRY:



SUM = A'B + AB'

CARRY = AB

LOGIC DIAGRAM:

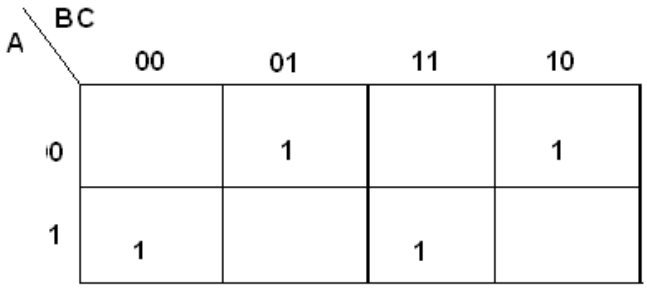


FULL ADDER

TRUTH TABLE:

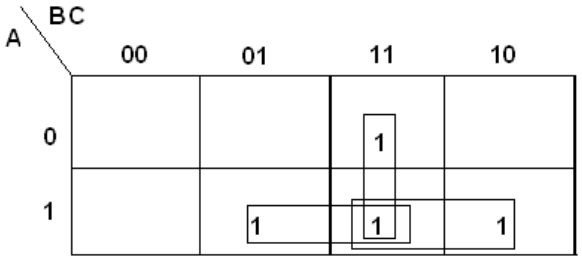
A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

K-Map for SUM:



SUM = A'B'C + A'BC' + ABC' + ABC

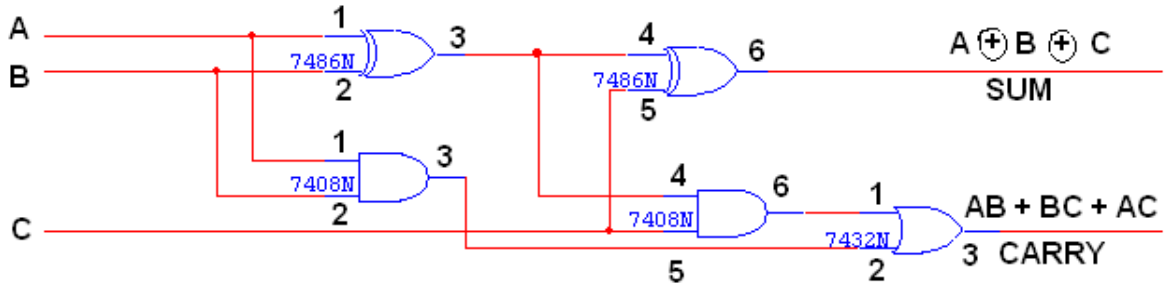
K-Map for CARRY:



CARRY = AB + BC + AC

LOGIC DIAGRAM:

FULL ADDER USING TWO HALF ADDER

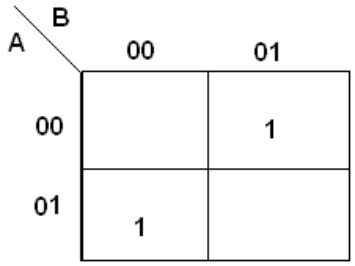


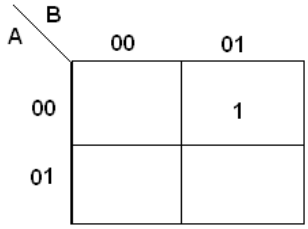
HALF SUBTRACTOR

TRUTH TABLE

A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

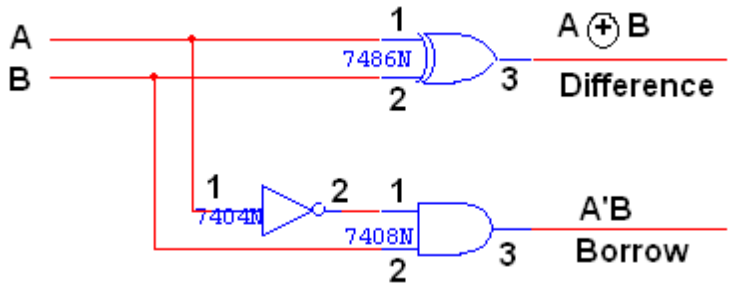
K-Map for DIFFERENCE: **K-Map for BORROW:**





DIFFERENCE = A'B + AB' **BORROW = A'B**

LOGIC DIAGRAM:

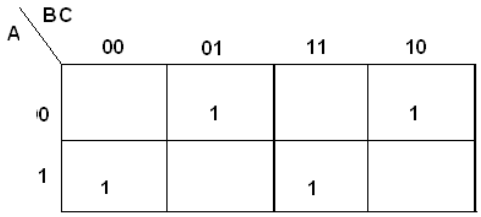


FULL SUBTRACTOR

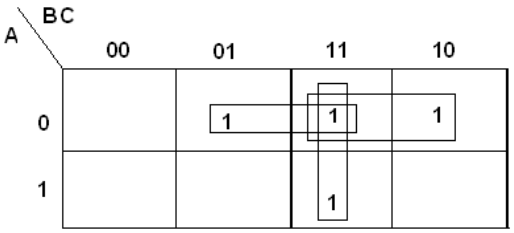
TRUTH TABLE:

A	B	C	BORROW	DIFFERENCE
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

K-Map for Difference:



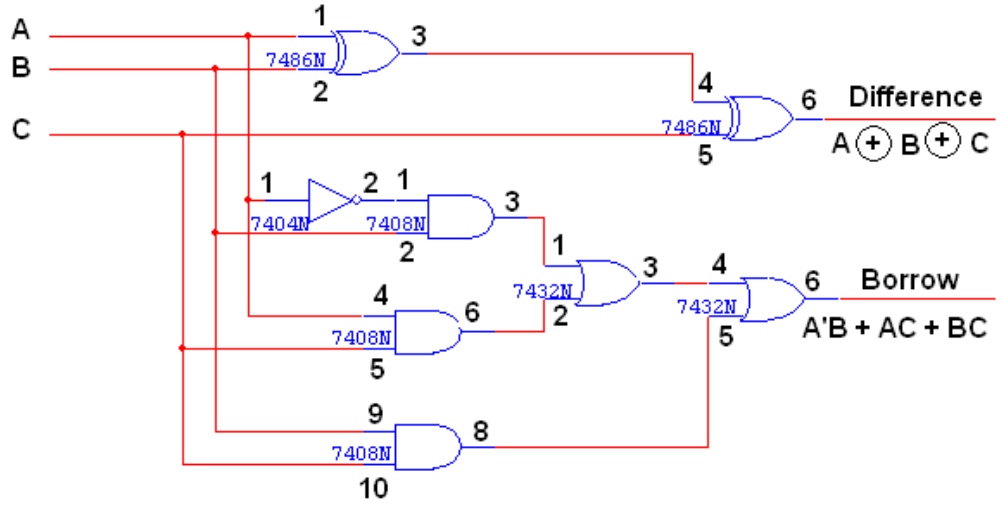
K-Map for Borrow:



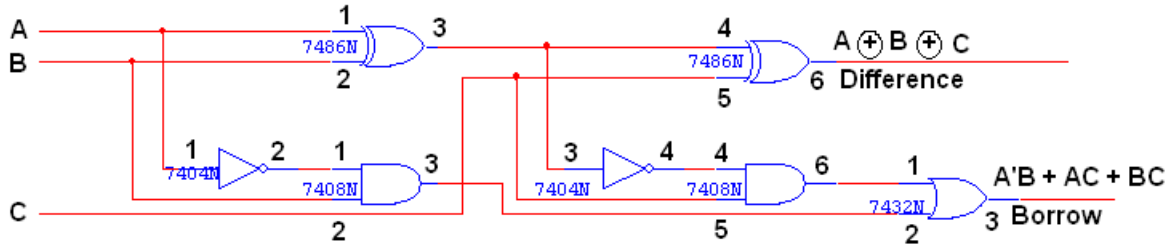
Difference = A'B'C + A'BC' + AB'C' + ABC

Borrow = A'B + BC + A'C

LOGIC DIAGRAM:



FULL SUBTRACTOR USING TWO HALF SUBTRACTOR:



6.4 Procedure:

a) Connections are given as per circuit diagram.

b) Logical inputs are given as per circuit diagram.

c) Observe the output and verify the truth table.

6.5 Conclusion:

Experiment no.: 07

7.1 Aim of the Experiment:

To design and implement multiplexer and demultiplexer using logic gates.

7.2 Apparatus required:

SL No.	COMPONENT	SPECIFICATION	QTY
1.	3 I/P AND GATE	IC 7411	1
2.	OR GATE	IC 7432	1
3.	NOT GATE	IC 7404	1
SL No.	**EQUIPMENT**	**SPECIFICATION**	**QTY**
1.	IC TRAINER KIT	-	1
2.	Patch Chords		AS REQUIRED

7.3 Theory:

MULTIPLEXER:

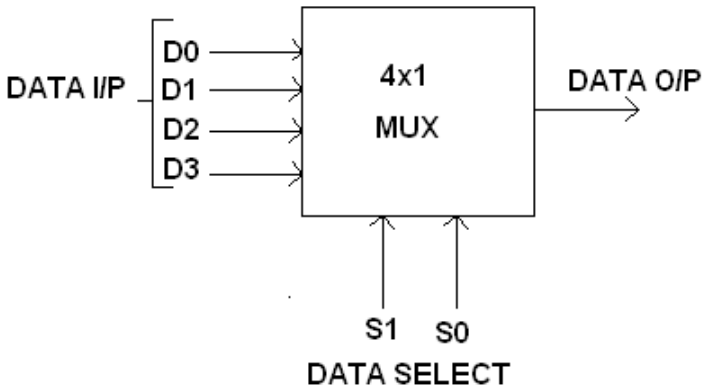
Multiplexer means transmitting a large number of information units over a smaller number of channels or lines. A digital multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally there are 2n input line and n selection lines whose bit combination determine which input is selected.

DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer.

In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND gates. The data select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:

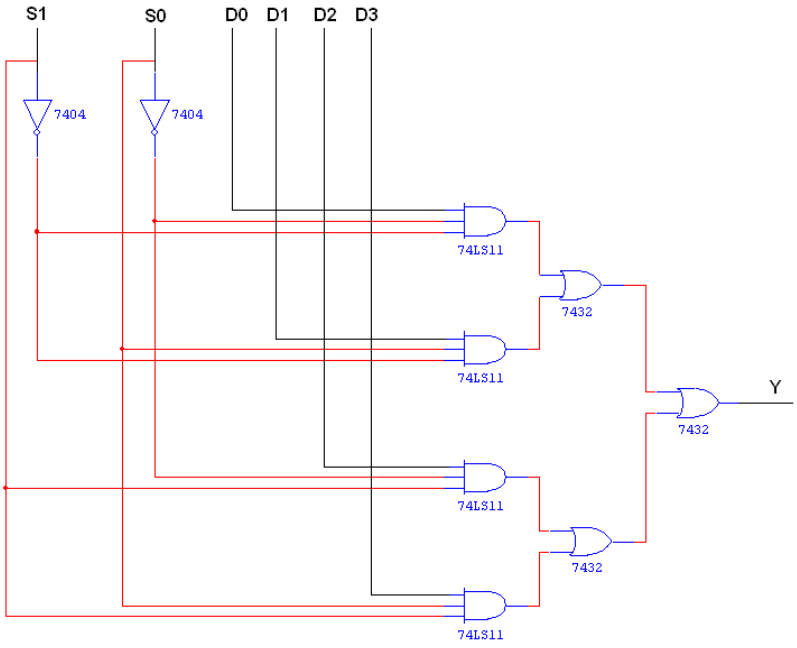


FUNCTION TABLE:

S0	S1	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

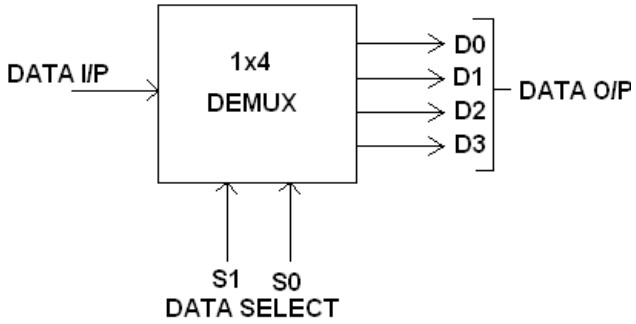
CIRCUIT DIAGRAM FOR MULTIPLEXER:



TRUTH TABLE:

S0	S1	Y =OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

BLOCK DIAGRAM FOR 1:4 DEMULTIPLEXER:

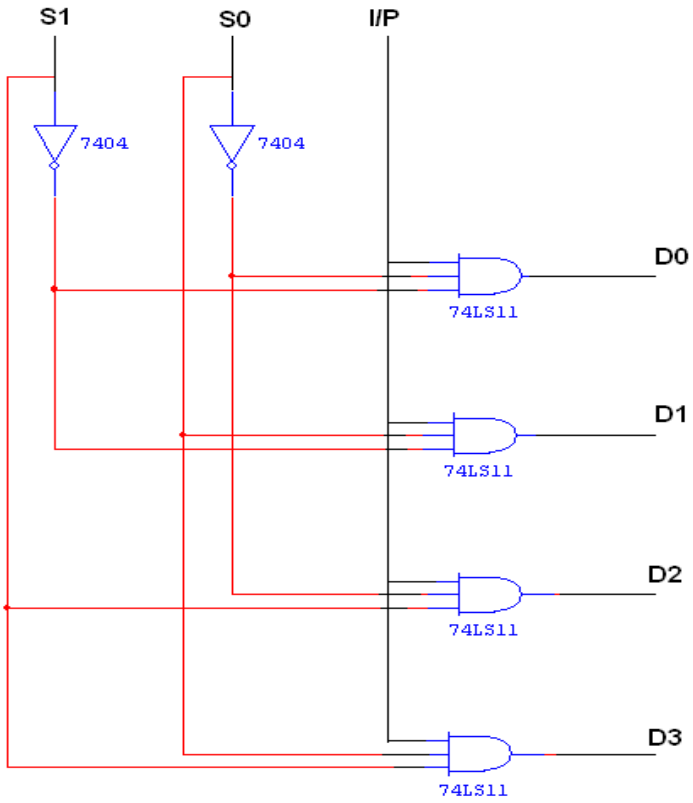


FUNCTION TABLE:

S0	S1	INPUT
0	0	**X → D0 = X S1' S0' '**
0	1	**X → D1 = X S1' S0**
1	0	**X → D2 = X S1 S0'**
1	1	**X → D3 = X S1 S0**

Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0

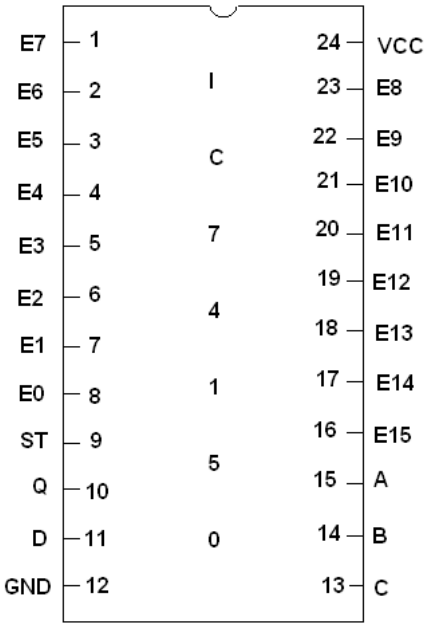
LOGIC DIAGRAM FOR DEMULTIPLEXER



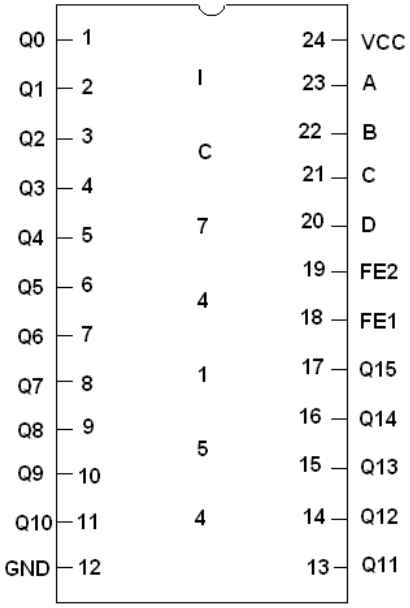
TRUTH TABLE:

INPUT			**OUTPUT**			
S1	S0	I/P	D0	D1	D2	D3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

PIN DIAGRAM FOR IC 74150:



PIN DIAGRAM FOR IC74154:



7.4 Procedure:

a) Connections are given as per circuit diagram.

b) Logical inputs are given as per circuit diagram.

c) Observe the output and verify the truth table.

7.5 Conclusion:

Experiment no.: 08

8.1 Aim of the Experiment:

Realization of S-R and J-K flip flop using 7400.

8.2 Apparatus required:

SL No.	COMPONENT	SPECIFICATION	QTY
1.	NOT GATE	IC 7404	1
2.	NAND GATE 2 I/P	IC 7400	1
3.	NOR GATE	IC 7402	1
SL No.	**EQUIPMENT**	**SPECIFICATION**	**QTY**
1.	IC TRAINER KIT	-	1
2.	Patch Chords		AS REQUIRED

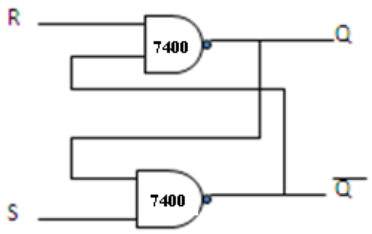
8.3 Theory

A Flip flop is a one bit storage device or memory element used to store binary information. It is also some times known as "Binary". A flip flop has two stable stages. The stable stages are '0' or '1'. It has two output i.e., normal or complimented (Q & Q'). Depending on the number of inputs and the way the output changes with respect to input they are divided into different types.

1. S-R Flip Flop
    a. Basic S-R Flip flop
    b. Clocked S-R Flip flop
2. J-K S-R Flip flop
3. Master J-K Flip flop
4. D- Flip flop
5. T- Flip flop

BASIC FLIP FLOP

LOGIC DIAGRAM:-

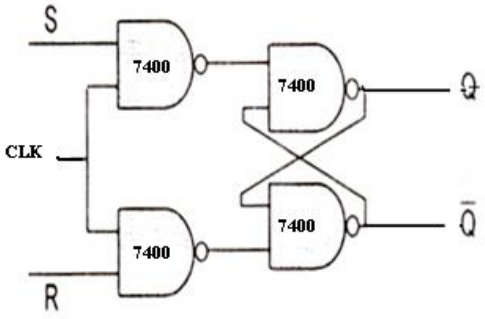


Truth Table

S	R	Q
0	0	Forbidden
0	1	1
1	0	0
1	1	No Change

R-S flip-flop using NAND gates

LOGIC DIAGRAM:-

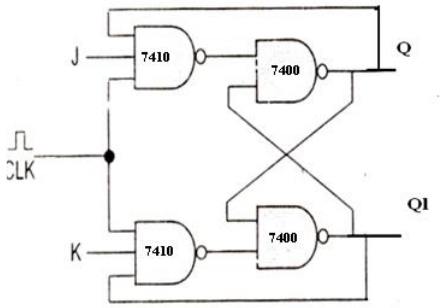


Truth Table

S	R	Q
0	0	No Change
0	1	1
1	0	0
1	1	Forbidden

J-k flip-flop using NAND gates

LOGIC DIAGRAM:-



Truth Table:-

S	R	Q
0	0	No Change
0	1	1
1	0	0
1	1	Race around

8.4 Procedure:

a) Connect the Flip-flop circuits as shown above.
b) Apply different combinations of inputs and observe the outputs.

8.5 Conclusion:

Experiment no.: 09

9.1 Aim of the Experiment:

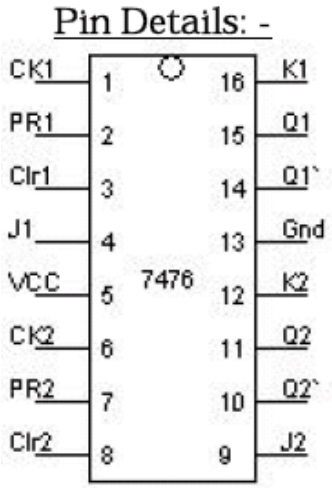
To design of 3-bit asynchronous counter and Mod-N counter.

9.2 Apparatus required:

SL No.	COMPONENT	SPECIFICATION	QTY
1.	J K Flip Flop	7476	2
2.	NAND GATE 2 I/P	IC 7400	1
3.	IC TRAINER KIT	-	1
4.	Patch Chords		AS REQUIRED

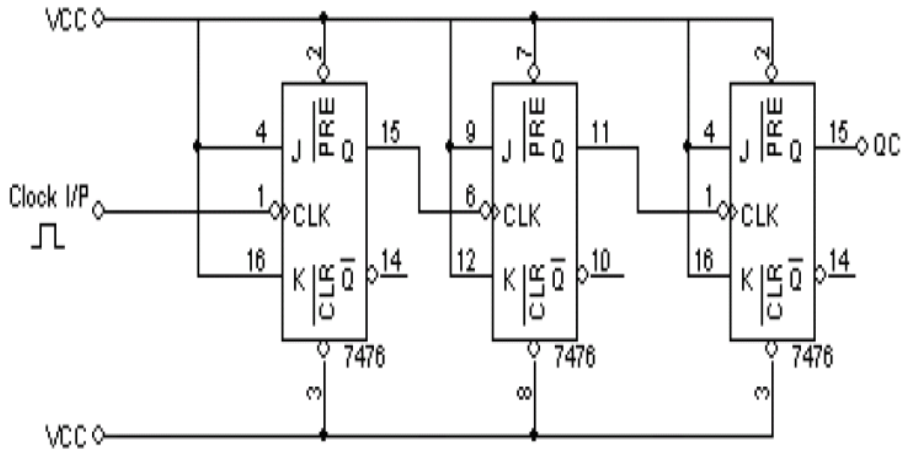
9.3 Theory:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. In synchronous common clock is given to all flip flop and in asynchronous first flip flop is clocked by external pulse and then each successive flip flop is clocked by Q or Q output of previous stage. A soon the clock of second stage is triggered by output of first stage. Because of inherent propagation delay time all flip flops are not activated at same time which results in asynchronous operation.

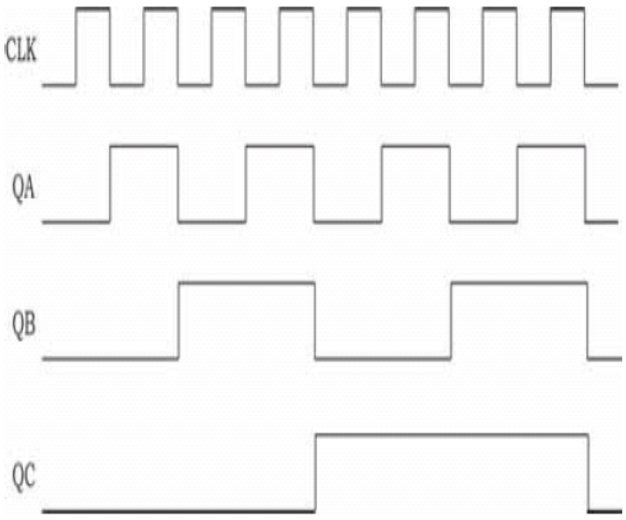


Logic Diagram

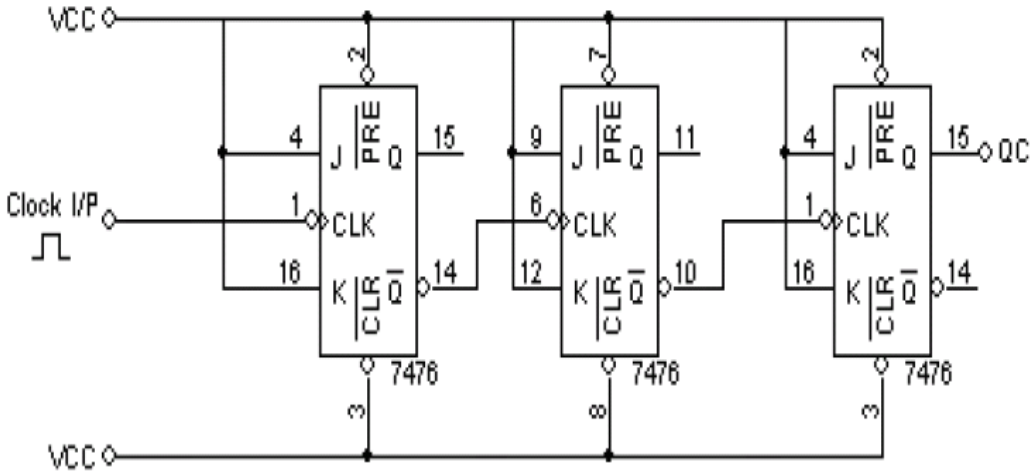
Circuit Diagram: - 3-Bit Asynchronous Up Counter



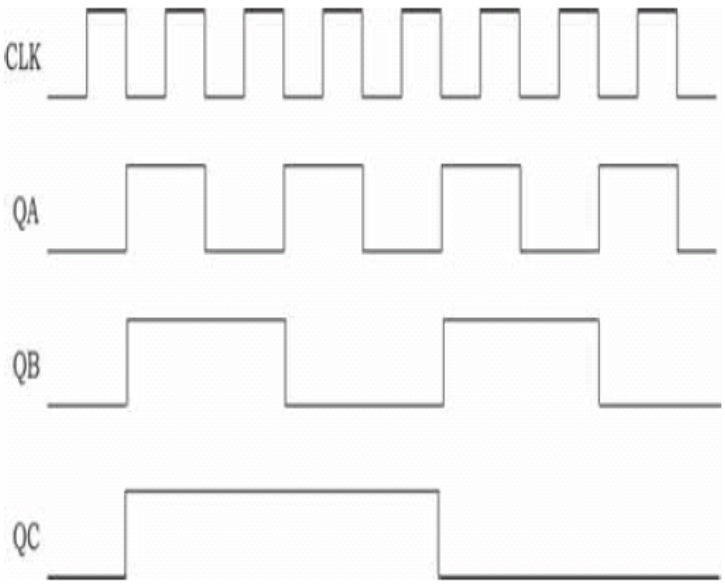
3-bit Asynchronous up counter			
Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0



Circuit Diagram: - 3-Bit Asynchronous Down Counter

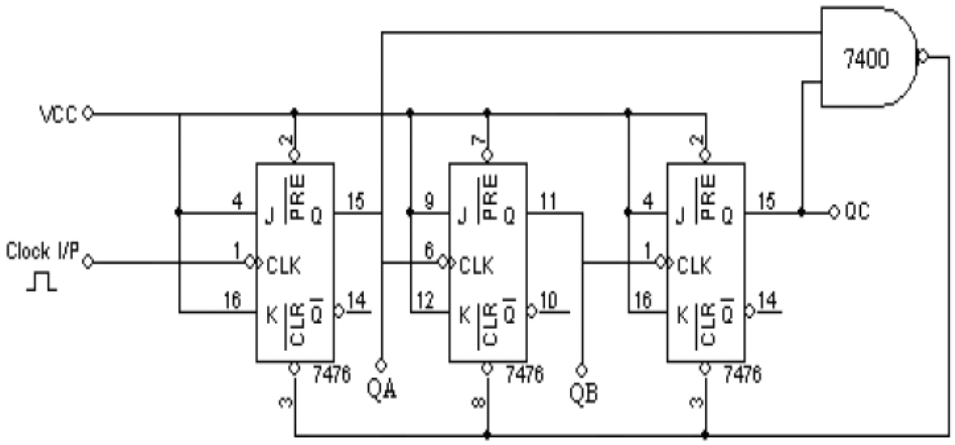


3-bit Asynchronous down counter			
Clock	QC	QB	QA
0	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
8	1	1	1
9	1	1	0

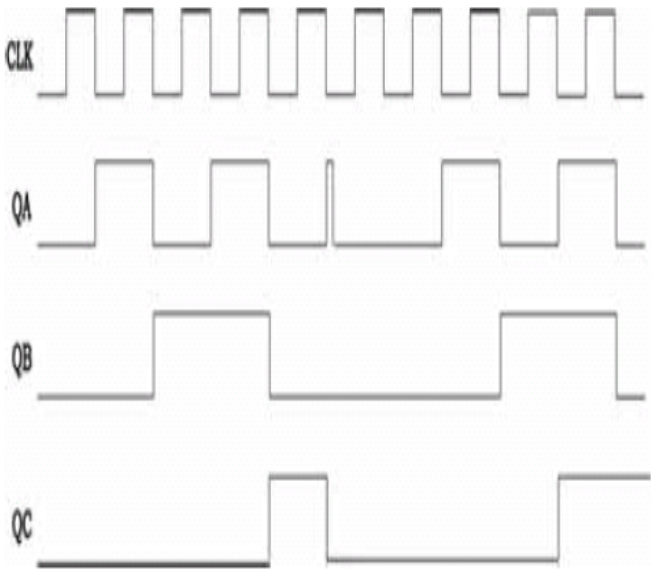


LOGIC DIAGRAM

Mod 5 Asynchronous Counter:-



Mod 5 Asynchronous counter			
Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0



9.4: Procedure:

a) Connections are made as per circuit diagram.

b) Clock pulses are applied one by one at the clock I/P and the O/P is observed at QA, QB & QC for IC 7476.

c) Verify the Truth table.

9.5 Conclusion:

Experiment no.: 10

10.1 Aim of the Experiment:

To design and implement

(i) Serial in serial out shift register
(ii) Serial in parallel out shift register
(iii) Parallel in serial out shift register
(iv) Parallel in parallel out shift register

10.2 Apparatus required:

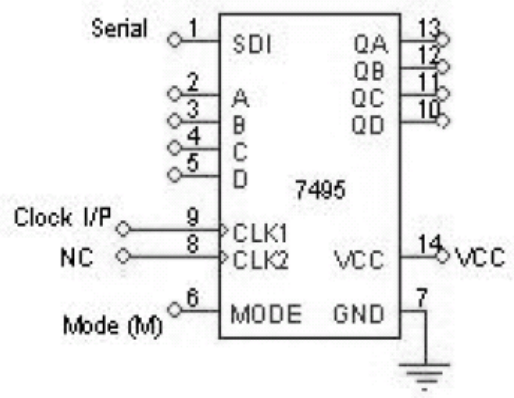
SL No.	COMPONENT	SPECIFICATION	QTY
1.	4 bit Register	IC 7495	1
SL No.	**EQUIPMENT**	**SPECIFICATION**	**QTY**
1.	IC TRAINER KIT	-	1
2.	Patch Chords		AS REQUIRED

10.3 Theory:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop. The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.

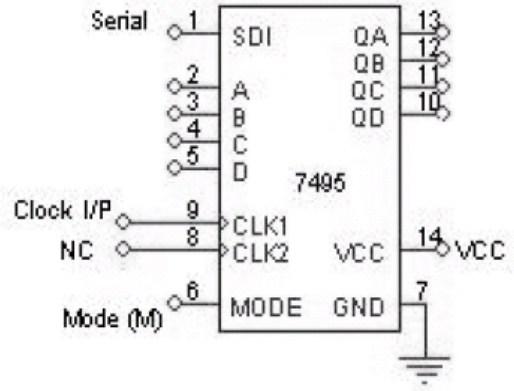
LOGIC DIAGRAM

SIPO (Right Shift):-



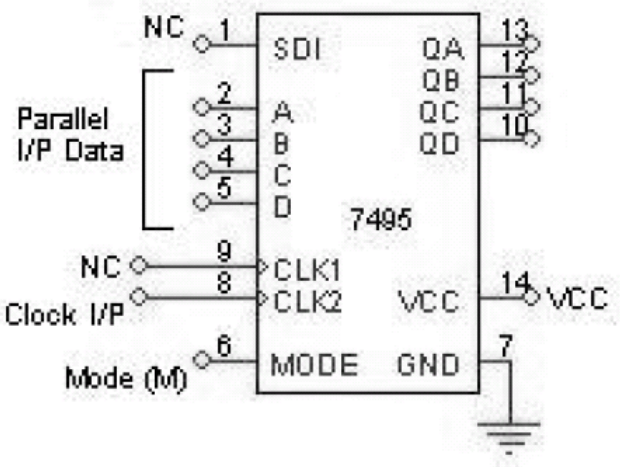
Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

SISO:-



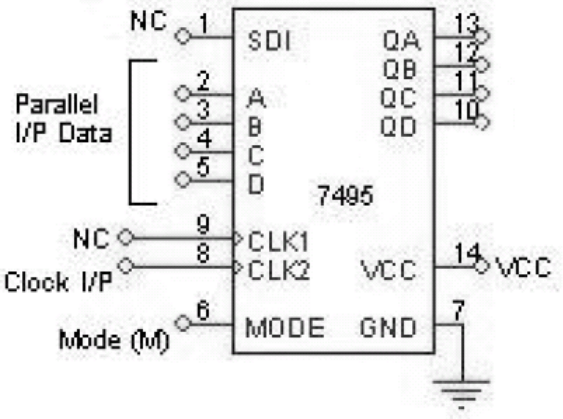
Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

PISO:-



Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

PIPO:-



Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

10.4 Procedure:

Serial In Parallel Out (SIPO):

1. Connections are made as per circuit diagram.
2. Apply the data at serial i/p
3. Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.
4. Apply the next data at serial i/p.
5. Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.
6. Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.

Serial In Serial Out (SISO):

1. Connections are made as per circuit diagram.
2. Load the shift register with 4 bits of data one by one serially.
3. At the end of 4th clock pulse the first data ‘d0’ appears at QD.
4. Apply another clock pulse; the second data ‘d1’ appears at QD.
5. Apply another clock pulse; the third data appears at QD.
6. Application of next clock pulse will enable the 4th data ‘d3’ to appear at QD. Thus the data applied serially at the input comes out serially at QD

Parallel In Serial Out (PISO):

1. Connections are made as per circuit diagram.
2. Apply the desired 4 bit data at A, B, C and D.
3. Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.
4. Now mode control M=0. Apply clock pulses one by one and observe the Data coming out serially at QD

Parallel In Parallel Out (PIPO):

1. Connections are made as per circuit diagram.
2. Apply the 4 bit data at A, B, C and D.
3. Apply one clock pulse at Clock 2 (Note: Mode control M=1).
4. The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.

10.5 Conclusion: